IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 6, Issue 2, February 2017

Design and Analysis of Track and Hold Circuit for Wireless Communication

Smita D. Waghmare[1], Dr. U. A. Kshirsagar[2]

P.G. Student, Electronics and Telecommunication Department, HVPM's College of Engineering and Technology, Amravati, India[1]

Professor & Head, Electronics and Telecommunication Department, HVPM's College of Engineering and Technology, Amravati, India[2]

Abstract: This Paper introduces conventional track and hold circuit using Microwind 3.1 VLSI Backnend Software A very fast and linear T & H circuit is the key element in any modern wideband data acquisition system. Applications like a cable-TV or a broad variety of different radio standards require high processing speeds with high resolution. The track-and-hold (T&H) circuit is a fundamental block for analog-to-digital (A/D) converters. Its use allows most dynamic errors of A/D converters to be reduced, especially those showing up when using high frequency input signals. This paper shows the result of module of conventional track and hold circuit made by using Microwind 3.1 VLSI Backend Software. It shows that the circuit consumes less power which is 9.083 uW. Chip area will also be less as the design technology is 32 nm.

Keywords: Track and Hold circuit, low power consumption, low chip area, sampling switch.

I. INTRODUCTION

Track and hold circuit is the fundamental block for anolog-to-digital converters (A/D). Its use allows most dynamic errors of A/D converters to be reduced, especially those showing up when using high frequency input signals. Track and hold circuit is inserted in front of a comparator array of a flash A/D converter to keep comparator's input voltages constant while the comparators are settling their output voltage levels. This Project includes different approaches for track and hold circuit.

This paper investigates effect of various design schemes and circuit topology for track-and-hold circuit to achieve acceptable linearly, high slew rate, low power consumption and low noise. Superior speed & acceptable linearity of source-followers makes it promising candidate for the purpose of this work.

II. LITERATURE REVIEW

From the rigorous review of related work and published literature it is observed that many researchers have designed different techniques for high speed communication in different techonologies. Since the real world today VLSI/CMOS very much in demand, from the careful study of reported work it is observed that track and hold circuit is the fundamental block for block for A to D converters. Its used for most dynamic errors of A to D converters to be reduced especially high frequency input signal.

A.N. Karanicolas, "A 2.7-V 300-MS/s track-and-hold amplifier," IEEE J. Solid-State Circuits, Dec,1997. In this Paper A.N. Karanicolas invented a fully differential bipolar track and hold amplifier(THA) employed an open-loop linearization technique compatible with low supply voltage. A feed through reduction method utilized the junction capacitance of a replica switch to provide a close match to the junction capacitance of the main switch.[1]

W. Yu, S. Sen and B. H. Leung, "Distortion Analysis of MOS Track-and-Hold Sampling Mixers Using Time-Varying Volterra Series",IEEE Transactions on circuits and systems-II: Analog and Digital Signal Processing, vol. 46, No. 2, Feb.1999. In this paper time-varying theory of Volterra series is developed and applied in the sampled-data domain to solve for harmonic and intermodulation distortion of a MOS-based track-and-hold sampling mixer with a nonzero fall-time LO waveform. Distortion due to sampling error is also calculated. These results, when combined with the continuous-time solution, quantify harmonic and intermodulation distortion of a track-and-hold type mixer completely. Closed form solutions are obtained. As a practical consequence, it is shown that for certain fall-time, the distortion of track-and-hold mixers can be better than what would be predicted by a simple application of time-invariant Volterra series theory.[2]

A. Boni, A. Pierazzi, and C. Morandi, "A 10-b 185-MS/s track-and-hold in 0.35-µm CMOS,"IEEE J. Solid-State Circuits,,Feb. 2001. This master paper described the design of a track-and-hold (T&H) circuit with 10bit resolution, 185MS/s. It is designed in a 0.35µm CMOS process. The circuit is supposed to work together with a 10bit pipelined analog to digital converter.[3]

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319 5940
International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 6, Issue 2, February 2017

Mohammad Hekmat and Vikram Garg, "Design and Analysis of a Source-Follower Track-and-Hold Circuit", EE315 (VLSI data conversion circuits), June 2006, this paper investigates effect of various design schemes and circuit topology for track and-hold circuit to achieve acceptable linearly, high slew rate, low power consumption and low noise.[4]

Takahide SATO†a), Member, Isamu MATSUMOTO, Nonmember,Shigetaka TAKAGI, Member, and Nobuo FUJII, Fellow, "Design of Low Power Track and Hold Circuit Based on Two Stage Structure",june 2008. In this paper, two track and hold circuits are designed and implemented using 65 nm CMOS technology. The first circuit is based on a dummy switch topology to decrease the charge injection error. The second circuit used a clock linearization technique to reduce the sampling instant inaccuracy. Simulation results showed that the track and hold circuit based on dummy transistor technique presented the best performances in terms of rapidity and accuracy.[5]

III. PROBLEM DEFINITION

Track and hold circuit is an important block used in Analog to Digital converter infront of array comparators to keep comparators input voltage constant.
Hence to design stable track and hold circuit is main task of our project proposal. Various design schemes and circuit topology will be investigated for track and hold circuit. Track and hold circuit will be design using 32 nm CMOS technology to acheive acceptable linearity and low noise.
Today, for high speed communication circuit power consumption is important parameter. Hence the problem definition of proposed project work is to design and analyze low power, low chip area track and hold circuit applicable for high speed communication.

IV. PROPOSED WORK

The circuit diagram of Track and Hold circuit is

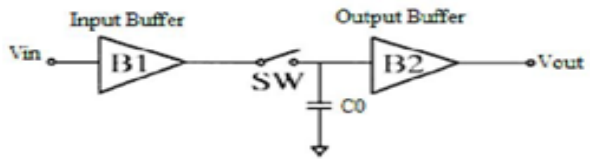


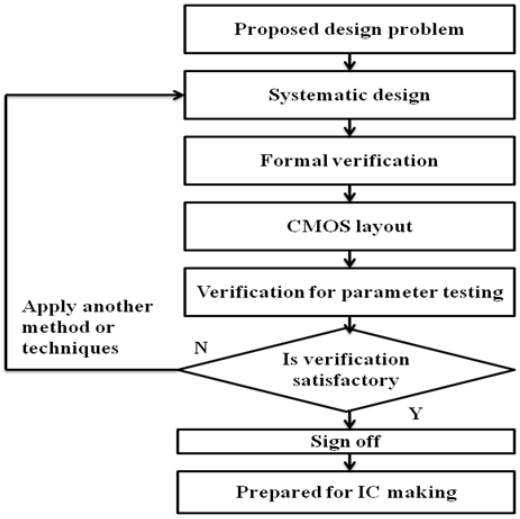
Figure: Circuit of Track and Hold circuit

The above circuit consist input and output buffer is simply connected by sampling switch
Track and hold circuit is a newly found fundamental circuit, whose behaviour is predicted by various design schemes and investigations of circuit topologies. Every step of design follows the design flow of Microwind 3.1 software. The design methodology will be according to VLSI design flow.

To achieve the proposed target following steps are included in the design and analysis of track and hold circuit.
1) Design of single MOS switch using 32 nm CMOS technology.
2) Design of Transmission gate using 32 nm CMOS technology.
3) Design of conventional track and hold circuit using source follower.
4) Design and analysis of track and hold circuit using transmission gate sampling switch.
5) Design and analysis of pseudo differential track and hold circuit
6) Design and analysis of fully differential track and hold circiuit.
7) Comparison of all track and hold circuit and their analysis.

V. DESIGN METHODOLOGY

The design methodology will be according to VLSI design flow.



Every step of design follows the design flow of Microwind 3.1 software.

Conventional T/H circuit:
A conventional source follower T/H circuit basically consists of input, output buffers, a switch and a sampling capacitor. An output buffer is usually used to charge and discharge the input capacitances of following comparators. A T/H circuit has two operation phases named "track phase" and "hold phase". During a track phase the switch is shorted and V_{out} becomes equal to V_{in}. On the other hand, during a hold phase the switch is opened and the T/H circuit keeps its output voltage equal to the value at end of track phase. A required hold time of a T/H circuit is usually decided by a settling time of the following comparators since the comparators must settle their output voltage during a hold time [9].

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 6, Issue 2, February 2017

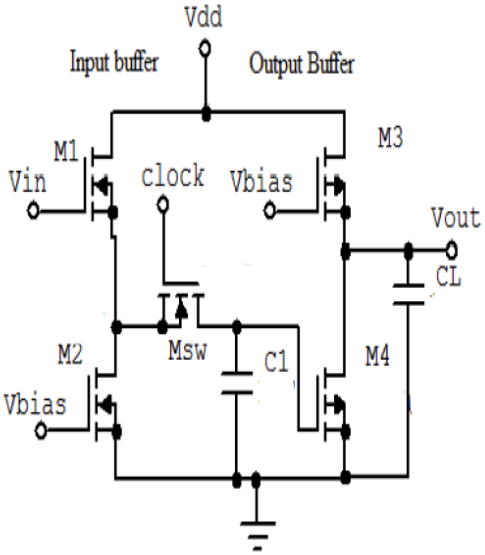
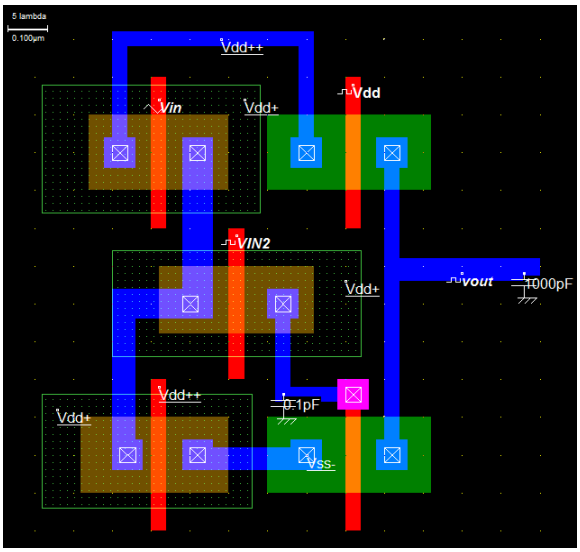


Figure. CMOS Design conventional T/H

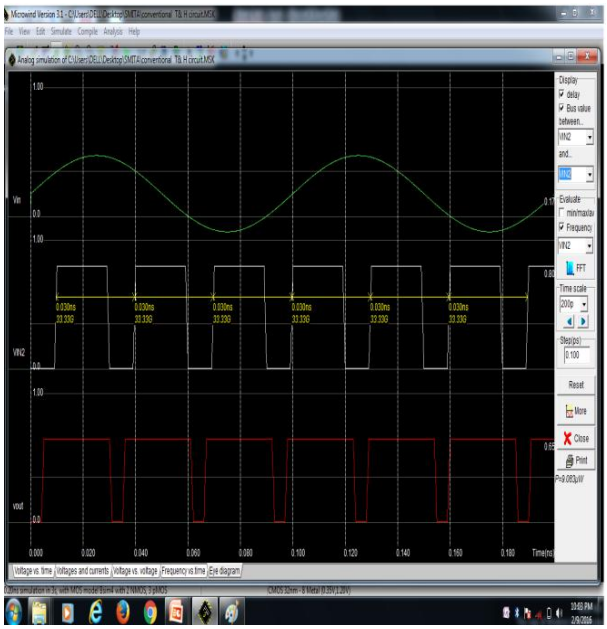
VLSI Design of Conventional T/H circuit:



Design specification of T/H circuit:

Cmos technology	32nm
Chip Area	Width: 5.1µm Height: 3.3 µm Surf: 16.8 µm
3 PMOS	P1 : 0.180×0.40 µm P2 : 0.200×0.040 µm P3 : 0.200×0.040 µm
2 NMOS	N1 : 0.200×0.40 µm N2 : 0.200×0.40 µm
Load Capacitance	1000 pf
Holding Capacitance	0.1 pf

Output Waveform of conventional T/H circuit:



Hspice simulation of conventional T/H circuit:

Power consumption	9.083 uW
Amplitude of Vin	0.4 v
Amplitude of VIN	0.80 v
Track time	0.020 ns
Hold time	0.04 ns

V. CONCLUSION

This paper resulted that the module of conventional track and hold circuit is made by using 32nm CMOS technology. The purpose of this work is to design a low-power track-and-hold circuit with a supply voltage of 0.8-1.2V. The above result showed that the power consumption is very low which is 9.083 uW where track time and hold time is 0.020 ns and 0.04 ns respectively.

REFERENCES

[1] "Study and Design of Low Drop-Out Regulators" by Gabriel Alfonso Rincon- Mora and Philip E. Allen, Department of Electrical and Computer Engineering, Georgia Institute of Technology.
[2] "CMOS Circuit Design, Layout and Simulation" by R. Jacob Baker, IEEE Press Series on Microelectronic Systems, Stuart K.Tewksbury and Joe E. Brewer, Series Editors.
[3] "A CMOS Capacitorless Low Drop-Out Voltage Regulator" by Vincent Lixiang Bu, Department of Electrical and Computer Engineering, Tufts University.
[4] "Full On-Chip CMOS Low DropVoltage Regulator" by Robert J. Milliken, Jose Silva-Martínez, Senior Member, IEEE, and Edgar Sánchez-Sinencio, Fellow, IEEE.
[5] "An Improved CMOS Error Amplifier Design for LDO Regulators in Communication Applications" by Xinquan Lai, Institute of Electronic CAD and Donglai Xu, School of Science and Technology.